

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)
Stephen W. Smith, et al.) Examiner:
Application No.:) Art Unit:
Filed: Herewith)
For: INTEGRATED MICROMACHINE RELAY)
FOR AUTOMATED TEST EQUIPMENT)
APPLICATIONS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

XXX 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

_____ A statement pursuant to 37 C.F.R. §1.97(e) or

_____ A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).

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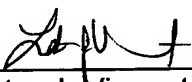
- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
- (2) A check for \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 16, 2003



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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	
				Filing Date	Herewith
				First Named Inventor:	Stephen W. Smith
				Art Unit	
				Examiner Name	
Sheet	1	of	5	Attorney Docket Number	53470P020D

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	3,609,991	10/5/1971	Chu et al.	
		US-	3,714,572	1/30/1973	Ham et al.	
		US-	3,882,691	5/13/1975	Baines et al.	
		US-	3,946,276	3/23/1976	Braun et al.	
		US-	4,044,396	8/23/1977	Haws et al.	
		US-	4,104,700	8/1/1978	Hutchison et al.	
		US-	4,109,707	8/29/1978	Wilson et al.	
		US-	4,138,643	2/6/1979	Beck et al.	
		US-	4,399,484	8/16/1983	Mayer	
		US-	4,698,728	10/6/1987	Tustaniwskyj et al.	
		US-	4,721,996	1/26/1988	Tustaniwskyj et al.	
		US-	4,782,290	11/1/1998	Sakai et al.	
		US-	4,791,983	12/20/1988	Nicol et al.	
		US-	4,809,134	2/25/1989	Tustaniwskyj et al.	
		US-	4,860,164	8/22/1989	Kaufman	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)			

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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		US-	4,865,123	9/12/1989	Kawashima et al.	
		US-	4,879,629	11/7/1989	Tustaniwskyj et al.	
		US-	4,938,279	7/3/1990	Betker	
		US-	4,989,070	1/29/1991	Iversen et al.	
		US-	5,048,599	9/17/1991	Tustaniwskyj et al.	
		US-	5,166,863	11/24/1992	Shmunis	
		US-	5,459,352	10/17/1995	Layton et al.	
		US-	5,818,246	10/6/1998	Zhong	
		US-	5,933,019	8/3/1999	Depue	
		US-	6,157,200	12/5/2000	Okayasu	
		US-	6,208,510 B1	3/27/2001	Trudeau et al.	
		US-	6,449,741 B1	9/10/2002	Organ et al.	
		US-				
		US-				
		US-				

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NON PATENT LITERATURE DOCUMENTS					
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		Wojciech Maly, "Current Testing," IEEE, 1990 International Test Conference, p. 257 (1990)			/
		S. Wayne Bolinger and Scott F. Midkiffs, "On Test Generation for IDDQ Testing of Bridging Faults in CMOS Circuits," IEEE, 1991 International Test Conference, pp. 598-607 (1991)			/
		E. Vandris and G. Sobelman, "A Mixed Functional/Iddq Testing Methodology for CMOS Transistor Faults," IEEE, 1991 International Test Conference, pp. 608-614 (1991)			/
		Chun-Hung Chen and Jacob A. Abraham, "High Quality Tests For Switch-Level Circuits Using Current and Logic Test Generation Algorithms," IEEE, 1991 International Test Conference, pp. 615-622 (1991)			/
		Robert C. Aitken, "Fault Location with Current Monitoring," IEEE, 1991 International Test Conference, pp. 623-632 (1991)			/
		Rohit Kapur, Jaehong Park, and M. Ray Mercer, "All Tests For A Fault Not Equally Valuable For Defect Detection," IEEE, 1991 International Test Conference, pp. 762-769 (1991)			/
		Ravi K. Gulati, Weiwei Mao, and Deepak K. Goel, "Detection of "undetectable" faults using IDDQ testing," IEEE, 1992 International Test Conference, pp. 770-775 (1992)			/
		Robert C. Aitken, "A Comparison of Defect Models for Fault Location with Iddq Measurements," IEEE, 1992 International Test Conference, pp. 778-787 (1992)			/
		Yukiya Muira and Kozo Kinoshita, "Circuit Design for Built-in Current Testing," IEEE, 1992 International Test Conference, pp. 873-881 (1992)			/
		R. Rodriguez-Montanes, E.M.J.G. Bruls and J. Figueras, "Bridging Defects Resistance Measurements in a CMOS Process," IEEE, 1992 International Test Conference, pp. 892-899 (1992)			/
		Kenneth M.. Wallquist, Alan W. Richter, and Charles F. Hawkins, "A General Purpose IDDQ Measurement Circuit," IEEE, 1993 International Test Conference, pp. 642-651 (1993)			/

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			Examiner Name		
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		Jerry M. Soden, Ronald R. Fritzmeier, and Charles F. Hawkins, "Zero Defects or Zero Stuck-At-Faults – CMOS IC Process Improvement, with IDDQ," IEEE, 1990 International Test Conference, pp. 255-256 (1990)	✓
		Keith Baker and Bas Verhelst, "IDDQ Testing Because "Zero Defects Isn't Enough": A Philips Perspective," IEEE, 1990 International Test Conference, pp. 253-254 (1990)	✓
		Steven McEuen, "WHY IDDQ?," IEEE, 1990 International Test Conference, p.252 (1990)	✓
		Charles Crapuchettes, "Testing CMOS on IDD on Large Devices," IEEE 1987 International Test Conference, pp 310-315 (1987)	✓
		Mike Keating and Dennis Meyer, "A New Approach To Dynamic IDD Testing," IEEE 1987 International Test Conference, pp 316-367 (1987)	✓
		Luther K. Horning, Jerry M. Soden, Ron R. Fritzemeier, and Charles F. Hawkins, "Measurements of Quiescent Power Supply Current for CMOS ICs in Production Testing," IEEE 1987 International Test Conference, pp. 300-309 (1987)	✓
		James T. Healy, "New CMOS Designs Demand Different and Radical Test Approaches," Electronic Test, Reprint, 5 pages (December 1985)	✓
		Hank Hogan, "More Than Toys," High Technology Careers Magazine, Feature Presentation, http://careerexpo.com/pub/dox197,micromachine197.html , 3 pages (1996)	✓
		"Micromachine Technology," http://www.info.hqs.cae.ntt.jp/RD/ACT_act_3/micromachine.html , 2 pages (prior to May 16, 2001)	✓
		LTX MicroMaster Plus Brochure (Prior to May 16, 2001) (USA)	
		LTX ValidMaster Plus Brochure (Prior to May 16, 2001) (USA)	

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		General Specifications, Class 388 and 283 Relays, http://magnecraft.com/page29.html , pgs. 1-2 (Wednesday, August 27, 1997)			/
		"General Purpose Square Base VDE Approved Relay," http://magnecraft.com/page33.html , pgs. 1-2 (Wednesday, August 27, 1997)			/
		LTX "Deltamaster Product Description," No. 999-7841-01-01, pp. 1-40 (LTX Corporation November 1992) (USA)			/
		"Fluorinert Liquid Heat Sink FC-3260," 3M New Product Announcement, January 1989			/
		Charles Wall, "Liquid Heat Sink Controls Computer Heat Flux," Reprinted from Electronic Packaging & Production (February 1989)			/
		Howard W. Markstein, "Liquid Cooling Optimizes Heat Transfer," Electronic Packaging and Production, pp. 46-49 (April 1988)			/
		Richard D. Danielson, Nick Krajewski, and Jerry Brost, "Cooling a Superfast Computer," Electronic Packaging and Production (July 1986)			/
		Ralph Remsburg, "New Routes to Cooler Electronics," Machine Design, pp. 73-76 (July 11, 1991)			/
		"Micromachined Relays," Teledyne Electronics and Communications, 1999.			
		J. Simon, S. Saffer, F. Sherman, and C.-J Kim, "Lateral Polysilicon Microrelays with a Mercury Micro-Drop Contact," pp. 1-15, 1998.			

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